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| 10/611,892 | 07/03/2003 | Howard E. Rhodes | M4065.0646/P646 | 3670 |

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| EXAMINER | |
|---|---|
| LANDAU, MATTHEW C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 02/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/611,892 | RHODES, HOWARD E. | |
| | Examiner | Art Unit | |
| | Matthew Landau | 2815 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,4-10,13-34,37-46,48 and 49* is/are pending in the application.

4a) Of the above claim(s) *23 and 44* is/are withdrawn from consideration.

5)☒ Claim(s) *1,4-7,9,10,13-20,26-34 and 37* is/are allowed.

6)☒ Claim(s) *21,22,24,25,38,43,45,46,48 and 49* is/are rejected.

7)☒ Claim(s) *40-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 November 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Claims 30 and 33 have been amended so as to read on the elected species. Claims 23 and 44 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention/species, there being no allowable generic or linking claim.

### *Drawings*

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the transfer transistor having a gate length greater than that of all other transistors (claims 5, 17, 31, and 32) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8 and 39 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 8, the limitation "and including said active area extension region" renders the claim indefinite. It is unclear what is meant by this limitation in the context of the claim, which states said active area extension region is spaced away from the transfer gate by a portion of a substrate *and including said active area extension region* (emphasis added). It appears the claim is stating the active area extension region is spaced from the gate by the active area extension region.

Regarding claim 39, the limitation "said single active area extension region and said halo implant being a part of said floating diffusion region" renders the claim indefinite. It is unclear what is meant by having the extension region and halo implant being "a part of" said floating diffusion region. Figure 1(a) of the instant application shows the floating diffusion region 28 is a separate region.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 21 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama et al. (US Pat. 6,166,405, hereinafter Kuriyama) in view of Komuro (US Pat. 5,780,902).

Regarding claim 21, Figure 5 of Kuriyama discloses a semiconductor substrate 30, a reset transistor (col. 11, lines 19-21) over said substrate; a photosensor 33 in electrical communication with said reset transistor, said photosensor being within said substrate on a first side of said reset transistor; a single active area extension region 34b in said substrate adjacent to said reset transistor, said single active area extension region being on a side of said reset transistor which is opposite to said first side; and an n-type layer 34a at the surface of said substrate and over said single active area extension region 34b. Note that a portion of region 34b extends beneath a portion of region 34a. Therefore, it can be considered region 34a is over region 34b. The difference between Kuriyama and the claimed invention is a halo implant below said single active area extension region and a threshold voltage adjustment implant in the channel region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region 14 formed in the channel (below an LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short

channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous.

Regarding claim 24, Figure 5 of Kuriyama discloses said photosensor 33 and said reset transistor are part of a transistor pixel circuit that further comprises a source follower transistor (amplification FET) and a row select transistor (select FET).

Claims 22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama in view of Komuro as applied to claim 21 above, and further in view of Choi et al. (US Pat. 5,793,088, hereinafter Choi).

Regarding claim 22, Figure 5 of Kuriyama discloses said reset transistor has a channel region (region beneath the gate). A further difference between Kuriyama and the claimed invention is said channel region having a threshold voltage adjustment implant. Figure 5 of Choi discloses a MOS transistor comprising a source/drain extension region 126, a halo implant region 120C, and a threshold voltage adjustment implant region 120A (col. 6, lines 25-28 and lines 39-49). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Kuriyama by additionally including a threshold voltage adjustment implant for the purpose of compensating for the edge effect associated with the halo implant and reducing junction capacitance (see abstract of Choi).

Regarding claim 25, Figure 5 of Kuriyama discloses the single active area extension region 34b is a lightly doped drain (col. 12, lines 3-6).

Claims 38, 43, and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuriyama in view of Komuro and Choi.

Regarding claim 38, Figure 1 of Kuriyama discloses a transistor in electrical contact with a photodiode 13 (col. 5, lines 66 and 67), said transistor comprising a single active area extension region 14b on a side of said transistor opposite from said photodiode, and a n-type layer 14a over said single active area extension region. Note that a portion of region 14b extends beneath a portion of region 14a. Therefore, it can be considered region 14a is over region 14b. A difference between Kuriyama and the claimed invention is a halo implant below said single active area extension region and a threshold voltage adjustment implant in the channel region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region 14 formed in the channel (below an LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous. A further difference between Kuriyama and the claimed invention is said channel region having a threshold voltage adjustment implant. Figure 5 of Choi discloses a MOS transistor comprising a source/drain extension region 126, a halo implant region 120C, and a threshold voltage adjustment implant region 120A (col. 6, lines 25-28 and lines 39-49). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was

made to further modify the invention of Kuriyama by additionally including a threshold voltage adjustment implant for the purpose of compensating for the edge effect associated with the halo implant and reducing junction capacitance (see abstract of Choi).

Regarding claim 43, the disclosure of Kuriyama does not explicitly disclose the image sensor is a CMOS imager. However, it would have been obvious to the ordinary artisan at the time the invention was made to use a CMOS imager as disclosed in the background of Kuriyama (col. 1, lines 18-25) for the purpose of integrating input elements with peripheral circuits on one chip.

Regarding claim 45, Figure 1 of Kuriyama discloses said transistor (charge transfer transistor) (col. 5, lines 20-24) is part of a pixel having at least two other transistors (reset and select transistors) in electrical communication with said photodiode 13.

Claims 46 and 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens in view of Kuriyama and Komuro.

Regarding claim 46, Figures 2 and 3 of Stevens disclose a pixel array, at least one pixel of said array comprising: a photoconversion device (photodiode) PD, and a first transistor gate 76 (transfer transistor) in electrical contact with said photoconversion device at a first side of said transistor gate, and said gate has a gate length which is increased relative to other transistors (RG and unlabeled transistor to the right of transistor 100). Note that the instant application defines the gate length as the distance labeled 44 in Figure 1(a) (see paragraph [0033]). It is clear that the corresponding feature in Figures 2 and 3 of Stevens is larger in the first transistor

TG than in the other two transistors indicated above. It is inherent that the pixel array of Kuriyama supplies signals to some type of image processor. A difference between Stevens and the claimed invention is said transistor gate having a single active area extension region (LDD region) on a second side of said transistor gate opposite said first side. Figure 1 of Kuriyama discloses a single active area extension region 14b (LDD region) on one side of a transfer transistor and a photodiode 13 (col. 5, lines 65-67) on the opposite side. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Stevens by including an active area extension region (LDD region) on the second side of the first transistor for the purpose of suppressing deterioration of the element properties (col. 6, lines 16-18 of Kuriyama). A further difference between Stevens and the claimed invention is a halo implant below said LDD region and a threshold voltage adjustment implant in the channel region. Figure 5C of Komuro discloses a MOS transistor with a halo implant region (threshold voltage implant) 14 formed in the channel (below an LDD region). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Stevens and Kuriyama by including a halo implant region as taught by Komuro for the purpose of suppressing the short channel effect and also the hot carrier generation (see abstract of Komuro). Although Komuro refers to region 14 as a pocket implant region, it is known in the art that terms "pocket" and "halo" are synonymous. It is also known that a halo (pocket) implant region affects the threshold voltage of a transistor. Therefore, it can be considered that the halo implant is also a threshold voltage adjustment implant. Note that it is considered that the "channel region" is the region between the source and drain.

Regarding claim 49, Figures 2 and 3 of Stevens disclose a source/drain region 80. Note that both the active area extension region and the source/drain region will be spaced away from the gate 76 by a portion 74 of a substrate 73/74 (Figure 3 of Stevens). Note that insulating film 74 can be considered to be part of the substrate.

Claim 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens in view of Kuriyama and Komuro, as applied to claim 46 above, and in further view of Choi.

Regarding claim 48, a further difference between Stevens and the claimed invention is a threshold voltage adjustment implant below a gate of said transistor. Figure 5 of Choi discloses a MOS transistor comprising a source/drain extension region 126, a halo implant region 120C, and a threshold voltage adjustment implant region 120A (col. 6, lines 25-28 and lines 39-49). In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to further modify the invention of Stevens by additionally including a threshold voltage adjustment implant for the purpose of compensating for the edge effect associated with the halo implant and reducing junction capacitance (see abstract of Choi).

***Allowable Subject Matter***

Claims 1, 4-7, 9, 10, 13-20, 26-34, and 37 are allowed.

Claims 40-42 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including said floating diffusion region is closer to said reset gate than to said transfer gate.

Regarding claim 15, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including an n-type doped region at the surface of said substrate and spanning said floating diffusion region and said single active area extension region.

Regarding claim 26, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including said floating diffusion region being closer to said reset gate than to said transfer transistor gate.

Regarding claim 32, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including said gate having a length which is greater than that of all other transistor gates of said pixel.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Response to Arguments***

Applicant's arguments filed November 29, 2005 have been fully considered but they are not persuasive.

Applicant argues that there would have been no motivation to combine the cited references for the purpose of the present obviousness rejection and that "There is simply nothing in either reference to suggest the desirability or utility of utilizing the transistor structure disclosed in Komuro with a photosensor structure like that disclose by Kuriyama et al.". This is not persuasive since the above rejection provides a specific motivation for the combination. It appears that Applicant is arguing the art is not analogous and therefore cannot be combined. However, both Kuriyama and Komuro disclose devices with MOS transistors. MOS transistors have certain problems, and those problems are the same regardless of the type of device in which it is used. Therefore, the art is analogous. Komuro teaches an advantage of having a halo/pocket implant in a MOS transistor. The advantage of the pocket implant of Komuro is common to all short channel transistors, including those in imaging devices. The fact that the transistor of Kuriyama is used in an imaging device does not mean the references cannot be combined. The specific type of device the transistors are used in is irrelevant. There is no reason why the features taught by Komura (specifically the pocket implant) cannot be incorporated into the transistor of Kuriyama. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge

gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971). In this case, the motivation to combine these references was taken directly from Komuro, and therefore is not improper hindsight.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on (571) 272-2298. The fax phone numbers for the organization where this application or proceeding is assigned are (571) 273-8300 for regular communications and (571) 273-8300 for After Final communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should any questions arise regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew C. Landau

February 8, 2006